BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/944,409	09/04/2001	Takchiro Shimizu	NITT.0039	1210

38327 7590 06/03/2004

REED SMITH LLP
3110 FAIRVIEW PARK DRIVE, SUITE 1400
FALLS CHURCH, VA 22042

EXAMINER	
MEONSKE, TONIA L	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/944,409	SHIMIZU ET AL.	
	Examiner	Art Unit	
	Tonia L Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/04/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in the Japan Patent Office on May 11, 2001. It is noted, however, that applicant may not have filed a certified copy of the 2000-340239 application as required by 35 U.S.C. 119(b) as the copy of the scanned image does not have a copy of a ribbon. Appropriate correction is required.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

3. The applicant or their representatives are urged to review the specification and submit corrections for all mistakes of a grammatical, clerical, or typographical nature. **For example,** the specification appears to be a literal translation into English from a foreign document and is replete with grammatical and idiomatic errors. Appropriate correction is required

Claim Objections

4. Claims 1-8 are objected to under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. The claims are generally narrative and indefinite, failing to conform with current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors. Appropriate correction is required

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-4 and 6-8 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Intel Corporation, IA-64 Application Developer's Architecture Guide, May 1999 (hereinafter referred to as Intel).

8. Referring to claim 1, Intel has taught a processor including an operation instruction comprising an instruction code (Pages 7-117, 7-130, and 7-131, mix1, mux1, mux2) and at least one register designating field (Pages 7-117, 7-130, and 7-131, GR r2), wherein the at least one register designating field is capable of designating a plurality of registers having consecutive numbers (Pages 7-117, 7-130, and 7-131, Register designating filed GR r2 designates eight consecutive registers.).

9. Referring to claim 2, Intel has taught a processor comprising:

a. a decoder designating a plurality of read registers in one field in an arbitrary number of register designating fields (Each instruction has an arbitrary number of register designating fields. Page 6-2, section 6.1.1, first bullet point); and

b. a register file for outputting data in a plurality of registers having consecutive numbers in accordance with an output from the decoder (Page 7-1).

10. Referring to claim 3, Intel has taught a processor comprising:

a. a decoder for designating a plurality of write registers in one field in an arbitrary number of register designating fields (Each instruction has an arbitrary number of register designating fields. Page 6-2, section 6.1.1, first bullet point); and

b. a register file capable of writing values in a plurality of registers having consecutive numbers in accordance with an output from the decoder (Page 7-1).

11. Referring to claim 4, Intel has taught the processor according to claim 2, as described above, and wherein the register file includes a plurality of banks, and by reading or writing data from the plurality of banks, the number of ports of reading or writing the data of the respective banks is restricted to be equal to or smaller than the number of the register designating fields, to thereby restrain an increase in a circuit scale caused by reading or writing the data by a number of times larger than the number of the fields (Page 7-117, The number of write ports is equal to the number of register designating fields. The last example has 2 write ports and two register designating fields.).

12. Referring to claim 6, Intel has taught the processor according to claim 1, as described above, and wherein a data pack operation, which is capable of dealing with a number of the data read from the read registers larger than a number of the data written to the write registers in order to read data from the registers larger in a number than the number of the read register designating fields, is realized without producing invalid portions in the write registers (Page 7-135, pack instruction).

13. Referring to claim 7, Intel has taught the processor according to claim 1, as described above, and wherein a data unpack operation, which is capable of dealing with a number of the data written to the write registers larger than a number of the data read from the read registers

such that the data can be written to the registers larger in a number than the number of the write register designating fields, is realized in parallel without executing data writing a plurality of times (Page 7-182, unpack instruction).

14. Referring to claim 8, Intel has taught the processor according to claim 1, as described above, and wherein an operation of outputting the data having a data width wider than a width of input data such that the data can be written to the registers larger in a number than the number of the write register designating fields, is realized without producing an invalid portion in the input data and without mounting a special register having a wider data width (Page 7-182, unpack instruction).

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Intel Corporation, IA-64 Application Developer's Architecture Guide, May 1999 (hereinafter referred to as Intel).

17. Referring to claim 5, Intel has taught the processor according to claim 1, as described above. Intel has not specifically taught wherein the number of the plurality of registers having the consecutive number is limited to the n-th power of 2 (n is a natural number), to thereby enable to reduce register selecting circuits. However, having the number of registers limited to the n-th power of 2 would maximize the efficiency of the wiring as none of the bit combinations would be wasted. Therefore it would have been obvious to one of ordinary skill in the art at the

time the invention was made to have the number of the plurality of registers having the consecutive number, as taught by Intel, be limited to the n-th power of 2 (n is a natural number), to thereby enable to reduce register selecting circuits, for the desirable purpose of maximizing the efficiency of the wiring as none of the bit combinations would be wasted.

Conclusion

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (703) 305-3993. The examiner can normally be reached on Monday-Friday, 8-4:30.

19. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

20. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100